AN1237: Si5332 Design Guidelines for Minimizing EMI

The Skyworks Si5332 any-frequency, low-jitter, family of clock generators has broad appeal in many different products and markets, including data center, communications, broadcast video, and automotive. Available in both standard industrial (–40 °C to +85C) as well as automotive (–40 °C to +105 °C) grade options, the Si5332 can consolidate entire clock trees into a single device, saving board space, BOM cost, and minimizing quartz elements to increase system reliability.

System designers are often challenged with mitigating radiated and conducted EMI in high-speed designs in order to meet recognized EMI/EMC standards, such as CISPR 25 and FCC Part15. This application note introduces features within the Si5332 as well as novel PCB design techniques that can be used to minimize EMI.

KEY FEATURES

- Clock termination guidelines for best signal performance and minimal EMI.
- Circuit design and PCB layout techniques for minimization of EMI.
- EMI test data using suggested guidelines showing real EMI improvements.

Table of Contents

1. Introduction

Designing products with EMI compliance in mind from the start is a much more efficient strategy than attempting to remediate compliance issues after a failing design has been built. This document provides design guidelines to help board-level circuit and PCB designers create EMI-optimized Si5332-based designs from the start, thereby increasing the likelihood of quickly securing required end-product EMI compliance certifications.

2. Clock Termination Guidelines

First, proper clock terminations, for both input and output clocks, are very important. Properly implemented clock termination supports both good signal integrity and EMI minimization. The following are some clock termination guidelines to consider:

For Differential Clock Formats

- Clock terminations are usually at the receiver end of transmission lines, unless format termination requirements dictate otherwise. Always keep terminations as close as possible to the respective end of a transmission line (i.e., keep source terminations as close as possible to the source, and, likewise, keep receiver terminations as close as possible to the receiver.)
- A balanced termination is required to keep currents on differential pairs symmetrically out of phase, thereby promoting good field cancellation. Use termination components (typically resistors) with 1% or better tolerance. Ensure that PCB traces are routed as differential pairs with matched trace lengths and constant impedance from end to end. Keep vias to an absolute minimum. Route all clocks before routing other PCB nets.

For LVCMOS Clocks

- LVCMOS receivers are typically high impedance inputs operating *without* receiver termination.
- It is important to match LVCMOS driver source impedance to PCB trace (transmission line) impedance. If driver source impedance is lower than PCB trace impedance a series termination resistor should be added. The value of the series source resistor should be chosen such that the driver source impedance plus series termination resistor is equal to PCB trace characteristic impedance. This series resistor should be placed as close as possible to the LVCMOS driver pin.

General Guidelines for Both Differential and LVCMOS

- Do not use a single Si5332 clock output to drive multiple clock receivers, regardless of driver format.
- Always consult the Si5332 Data Sheet and/or the Si5332 Reference Manual for Si5332 specific input and output clock termination requirements. Do not assume Si5332 termination requirements are the same as other products or devices. Termination requirements often vary from product to product. Ensure that proper clock terminations are in place.

3. General Clock Routing Guidelines for EMI Reduction

Clock signal routing can have the greatest impact on EMI reduction. Improper layout can result in a product that is virtually impossible to pass EMI compliance testing. Observing the following recommended layout design guidelines will help ensure your PCB layout supports best practices for EMI reduction.

- Route **all** clocks using **Stripline** techniques (see example layout in 6.1 Example EMI Test Board Clock Routing Details).
- Perform all clock routing first to get best routing. Use 45 degree or curved turns only. **Keep differential pairs length matched** to avoid path delay skew.
- Use impedance-controlled routing for **all** clocks, both differential and single-ended. Typically, 100 Ω (or 85 Ω) differential, 50 Ω (or 42.5 Ω) single-ended.
- Use ground stitching vias to connect the ground planes along Stripline clock path on outside of differential pair (see example layout in section 6.1 Example EMI Test Board Clock Routing Details).
- Keep the ground path between clock driver and receiver solid. Do not allow isolation cuts to separate the ground return path. Envision the Stripline clock path, including ground layers above and below the clock traces, as a continuous “tunnel” from driver to receiver that can’t be violated.
- Keep other signals as far away as possible or isolated from clock traces. If there is any potential for crosstalk from another signal on the same layer, use isolation grounds if required, but keep clock trace impedance constant. (i.e., there should be no clock trace impedance discontinuities due to other signal or isolation ground runs).

4. LVCMOS-Specific Clock Routing Guidelines

Single-ended LVCMOS clocks are notorious for being a source of EMI. For maximum reduction of EMI inherent in LVCMOS clocks, the following techniques are highly recommended:

Configure all LVCMOS Clock Drivers as Complementary

- In ClockBuilder Pro, choose the “LVCMOS Comp.” driver type, and route both signals exactly as would be done for a differential pair, following the same routing rules as for true differential clocks.

- Use one side of the complementary LVCMOS pair as the intended LVCMOS clock.
- Terminate the unused side of the pair as close as possible to the actual clock input with a capacitor to ground. The capacitor value must be the same as the receiving device’s clock input capacitance. Choosing the proper value for this capacitor is important to balance the dynamic currents on each side of the “differential” pair.

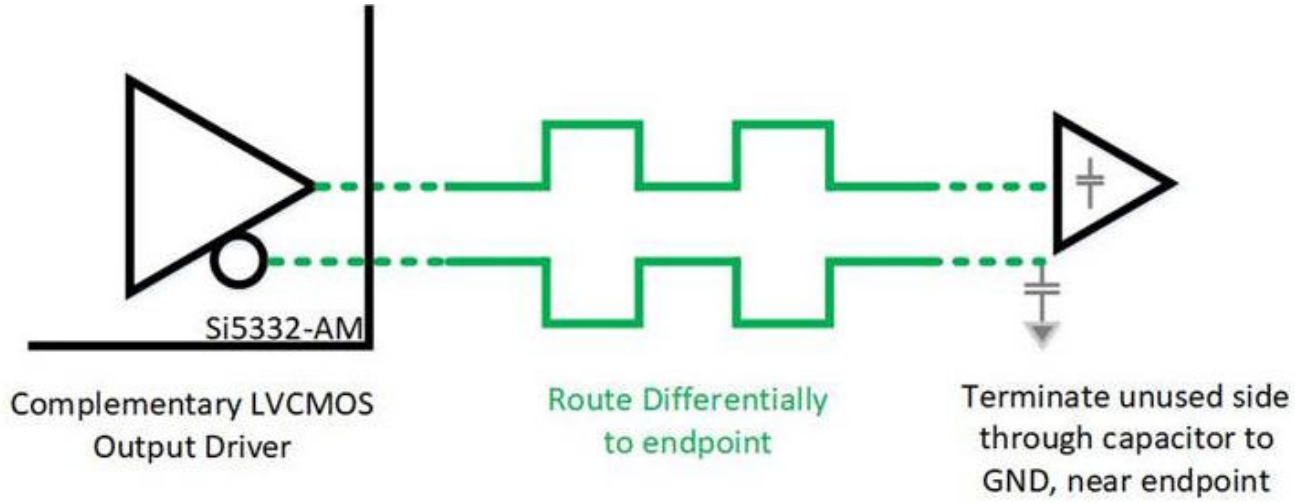


Figure 4.1. Complementary LVCMOS Clock Routing and Termination

5. Use of Balanced Differential Clocks Plus Stripline Routing is Best EMI Reduction Solution

There are many sources describing how the use of differential clocks can reduce EMI, but the key is having the differential pair implemented as a truly balanced differential pair, as described in earlier clock termination guidelines.

See http://www.emcs.org/acstrial/newsletters/summer10/DesignTips.html for more information about why truly balanced differential pairs are best. Length matching (minimizing skew) and balanced loading (for matching rise/fall times and amplitudes) is very important to minimize EMI.

Even the best attempt at ensuring the differential pair is truly balanced can still result in some amount of radiated EMI components due to common mode radiation effects. In this EMI study: http://www.sigcon.com/Pubs/edn/ReducingEMI.htm, you can learn how common mode radiation can reduce the effectiveness of a differential-only EMI reduction solution.

Both studies point out how common mode radiation issues can become a factor when using simple Microstrip layouts, even if differential signals are used. This is the primary reason why using **Stripline** techniques is recommended instead of Microstrip. Stripline layout can contain residual common-mode EMI as well as any differential field imbalance EMI. By combining Stripline clock routing, which provides Faraday cage shielding within the PCB, with truly balanced differential signal field cancellation, the best of both solutions can be realized.

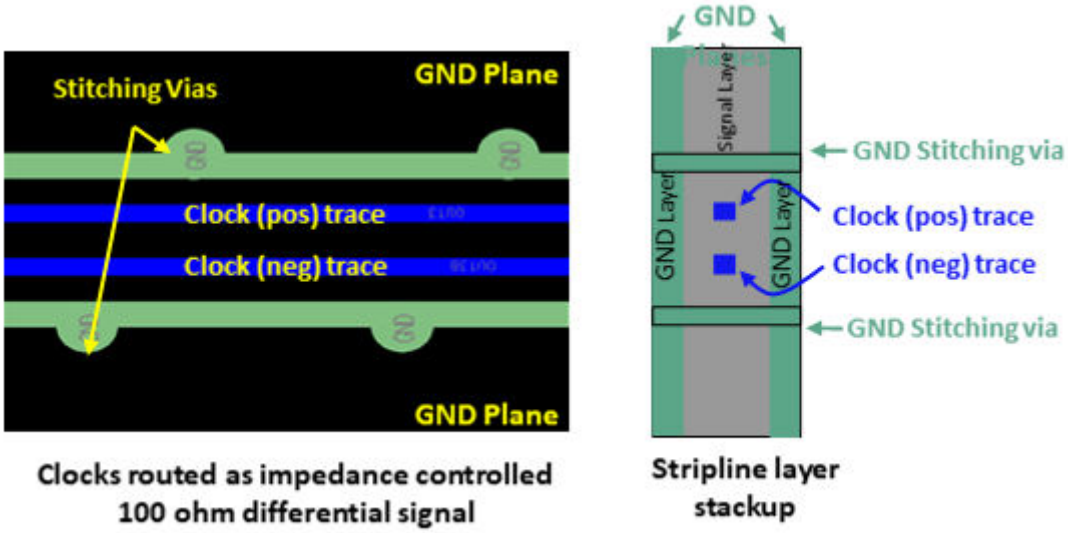


Figure 5.1. Example Stripline Clock Routing

6. Example EMI Test Board and EMI Test Data

To test and validate the suggested design/layout techniques presented in this document, Skyworks has developed the Si5332QFN40-AM2-AUTO-EVB evaluation board to represent a “real world” test platform. This PCB test platform consists of the following:

- Si5332-AM2, 8-output clock generator positioned in the middle of the PCB.
- Eight clock outputs (combination of LVCMOS and LVDS) routed as balanced differential signals from the clock generator to endpoints near the perimeter of the PCB.
- Clock traces were routed in various lengths (2.55” to 6.14”) in serpentine fashion to emulate real-world design requirements.
- Clocks were routed using a Stripline technique and terminated as required at the header endpoint.

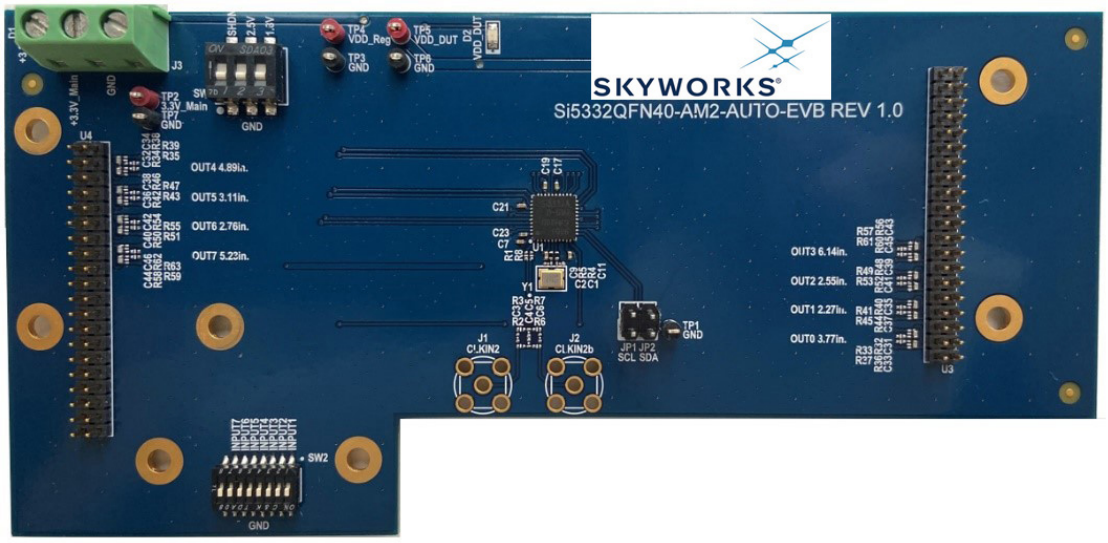


Figure 6.1. Example EMI Test Board and EMI Test Data

The above Si5332 test board was designed to fit within an automotive infotainment chassis enclosure (shown below), with the Si5532 test board being the only active circuit within the enclosure. This board and enclosure were tested for CISPR 25 EMI compliance to determine the level of radiated emissions due to the Si5332 clock generator test board independently of other emission sources.

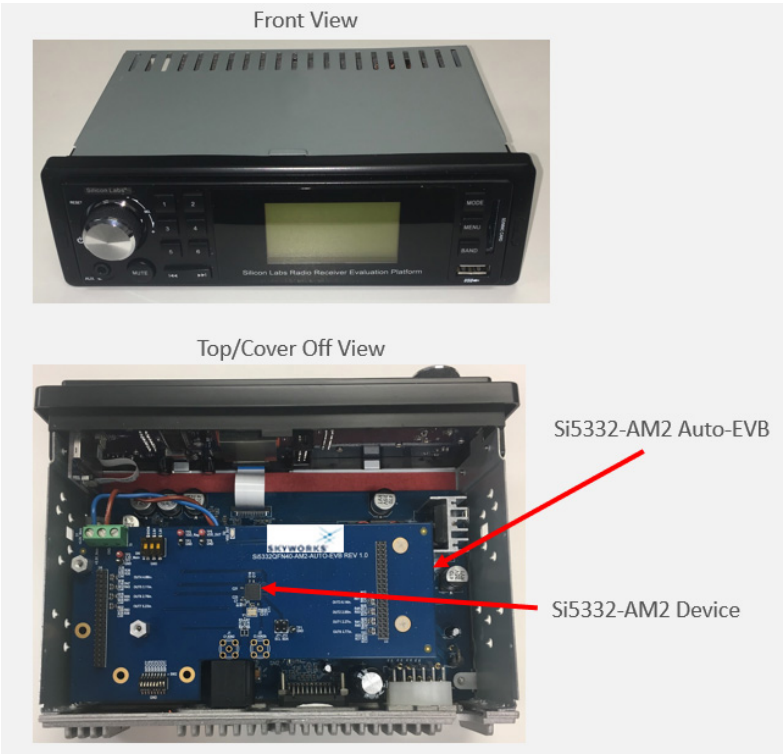


Figure 6.2. Automotive Style Enclosure

6.1 Example EMI Test Board Clock Routing Details

The images below provide a more detailed overview of the Si5332-QFN40-AM1-Auto-EVB board's clock signal layout. The clocks are routed using various lengths and paths towards the headers. The headers are used to simulate device pin loading. The required clock end point terminations can be seen immediately adjacent to the headers at the end of clock traces. Four clocks are routed to left header and four clocks to the right header. All clocks were routed using 100-ohm impedance controlled differential rules. The expanded views below show more detail of the Stripline layer stack-up and stitching vias connecting the ground layers above and below the differential clocks.

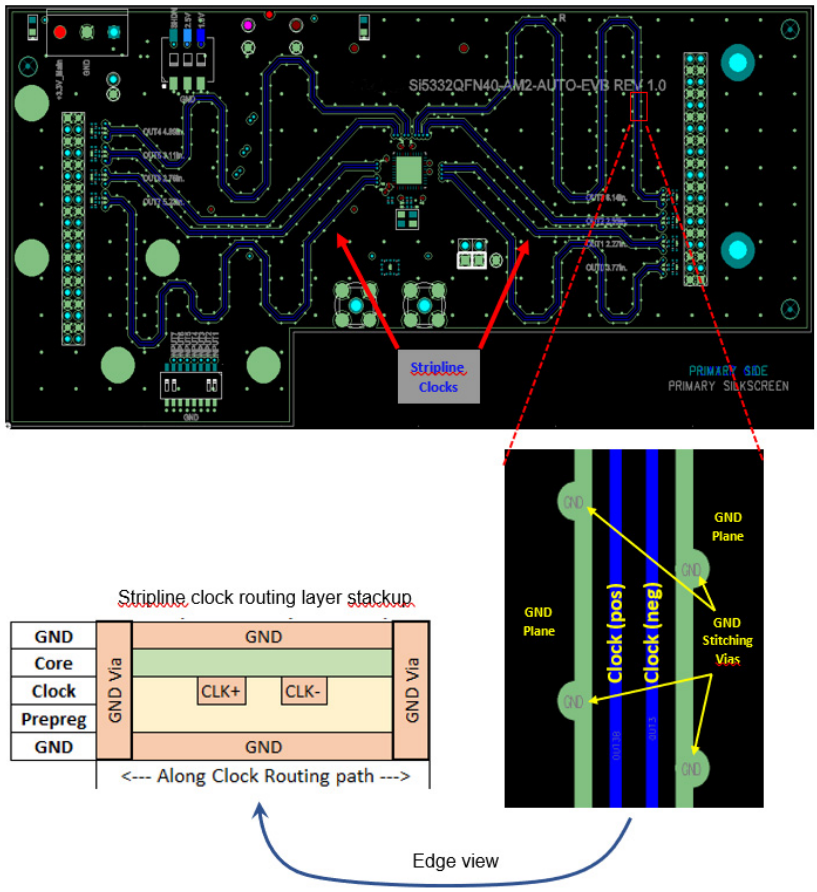


Figure 6.3. Stripline Layer Stackup of the Clock Layers

For testing details showing the specific effectiveness of the various EMI reduction techniques described in sections 2 through 6, refer to 9. Appendix—Prior EMI Test Data Demonstrating Effectiveness of Suggested EMI Techniques.

7. Full Independent Lab Testing—CISPR 25 Class 5 Emissions Test Results

The Si5332QFN40-AM2-AUTO-EVB board and enclosure, shown in Figure 6.2 Automotive Style Enclosure on page 8, was sent to Elite Engineering, a well-known EMI/EMC test lab, to undergo CISPR 25 Class 5 EMI testing. The Si5332QFN40-AM2-AUTO-EVB was submitted for CISPR 25 Class 5 EMI testing using the output frequency profile shown in the following table, which is based on a real-world system frequency profile.

Table 7.1. Si5332-AM2 Output Frequency Profile for CISPR 25 Class 5 EMI Testing

Si5332-AM2 CISPR 25 Testing - Output Profile		
Clock	**Frequency**	**Format**
OUT0	100 MHz	LVDS 3.3 V
OUT1	156.25 MHz	LVDS 3.3 V
OUT2	125 MHz	LVDS 3.3 V
OUT3	Unused	Unused
OUT4	50 MHz	LVDS 3.3 V
OUT5	25 MHz	LVCMOS comp, 3.3 V, 50 Ω
OUT6	26 MHz	LVCMOS comp, 3.3 V, 50 Ω
OUT7	Unused	Unused

The Si5332QFN40-AM2-AUTO-EVB passed all CISPR 25 Class 5 tests for radiated and conducted emissions, the details of which are shown in 7.1 Radiated Emissions Test Results.

7.1 Radiated Emissions Test Results

Shown below are CISPR 25 Class 5 test results for Si5332QFN40-AM2-AUTO-EVB Radiated and Conducted Emissions showing full compliance.

Note: Please note that effective July 26, 2021, the former Infrastructure and Automotive business of Skyworks is now part of Skyworks' Mixed Signal Solutions. All Skyworks registered trademarks that may be contained herein remain the sole property of Skyworks Solutions, Inc. and are only for nominative descriptive purposes and do not represent any sponsorship or endorsement of such product(s) by Skyworks.

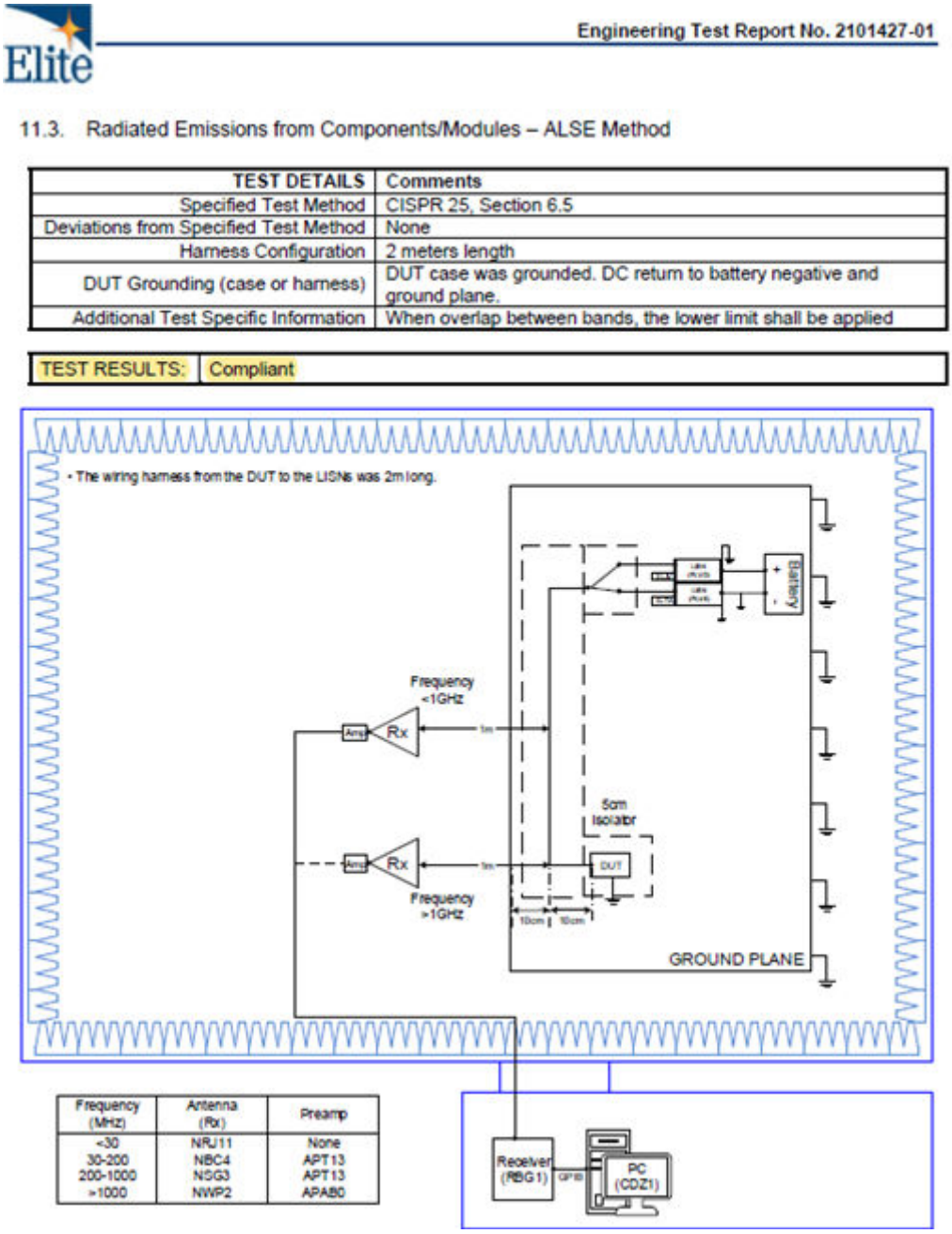
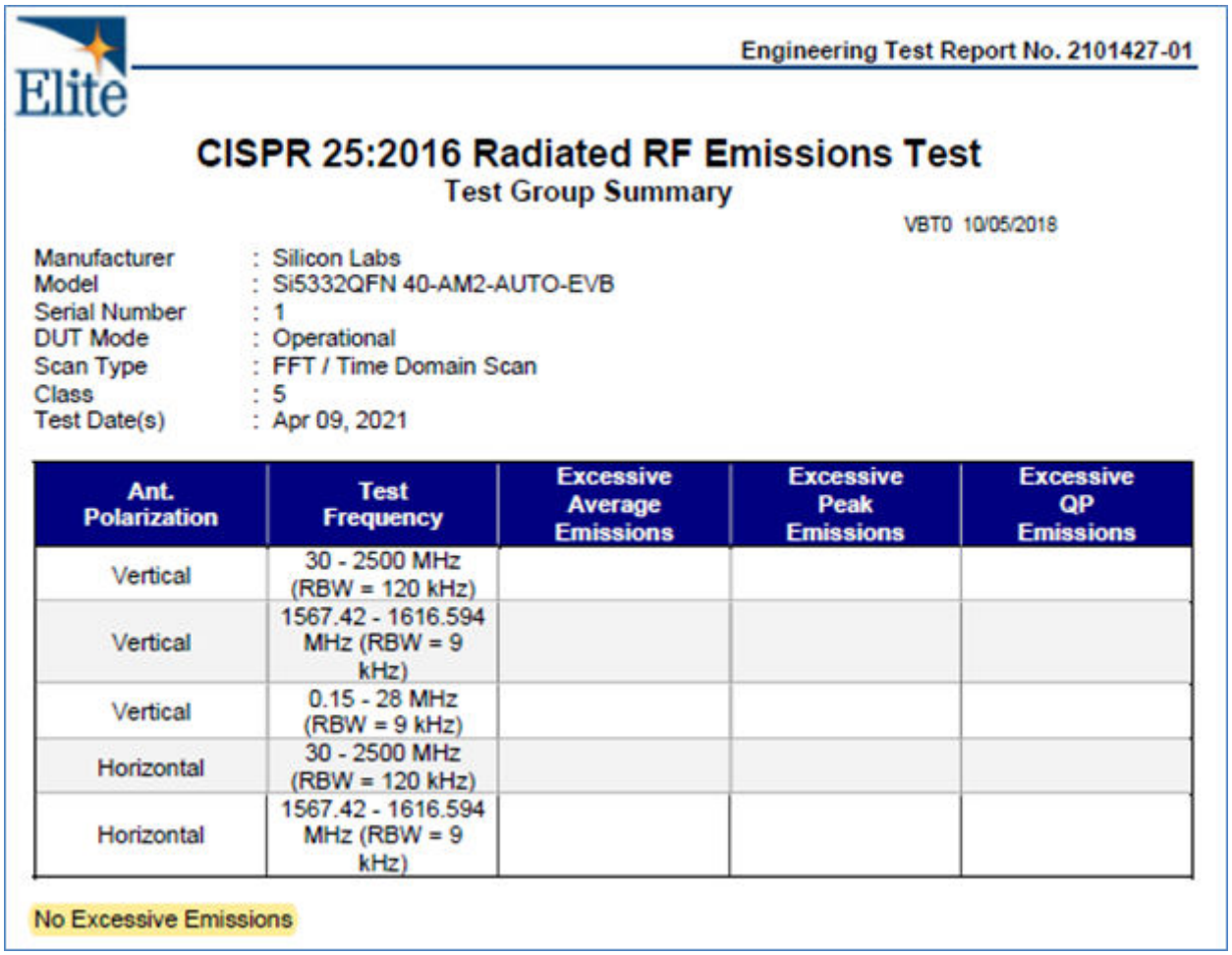


Figure 7.1. Radiated Emissions from Components/Modules—ALSE Method Test Setup Diagram



Engineering Test Report No. 2101427-01

CISPR 25:2016 Radiated RF Emissions Test

Test Group Summary

VBT0 10/05/2018

Manufacturer : Silicon Labs
Model : Si5332QFN 40-AM2-AUTO-EVB
Serial Number : 1
DUT Mode : Operational
Scan Type : FFT / Time Domain Scan
Class : 5
Test Date(s) : Apr 09, 2021

Ant. Polarization	Test Frequency	Excessive Average Emissions	Excessive Peak Emissions	Excessive QP Emissions
Vertical	30 - 2500 MHz (RBW = 120 kHz)			
Vertical	1567.42 - 1616.594 MHz (RBW = 9 kHz)			
Vertical	0.15 - 28 MHz (RBW = 9 kHz)			
Horizontal	30 - 2500 MHz (RBW = 120 kHz)			
Horizontal	1567.42 - 1616.594 MHz (RBW = 9 kHz)			

No Excessive Emissions

Figure 7.2. Radiated RF Emissions Test Summary

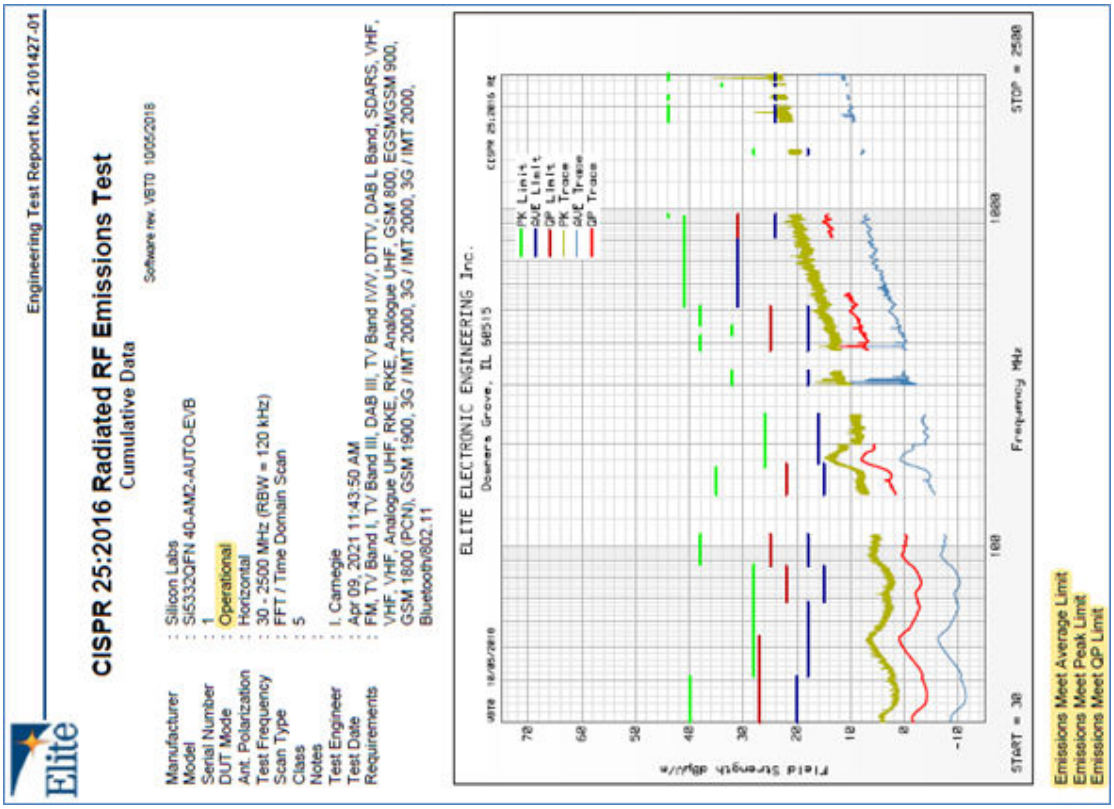


Figure 7.3. DUT Operational - Horizontal RF Emissions

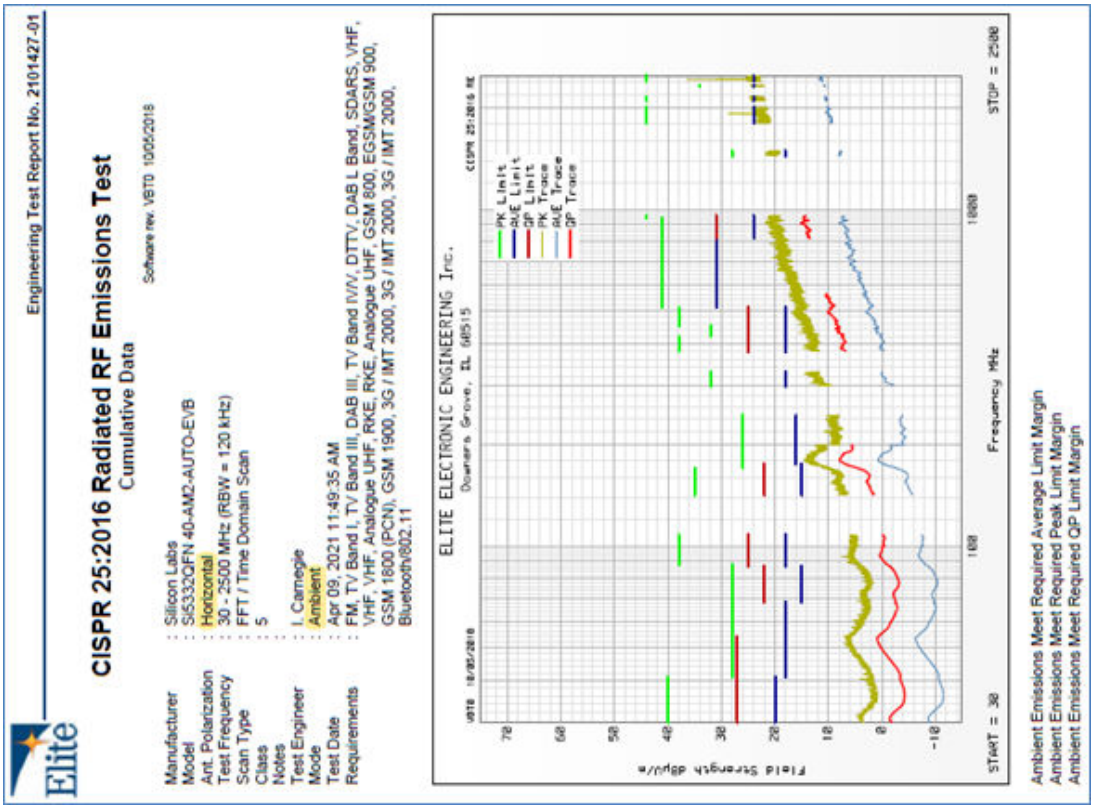


Figure 7.4. DUT Power Off - Horizontal Background RF

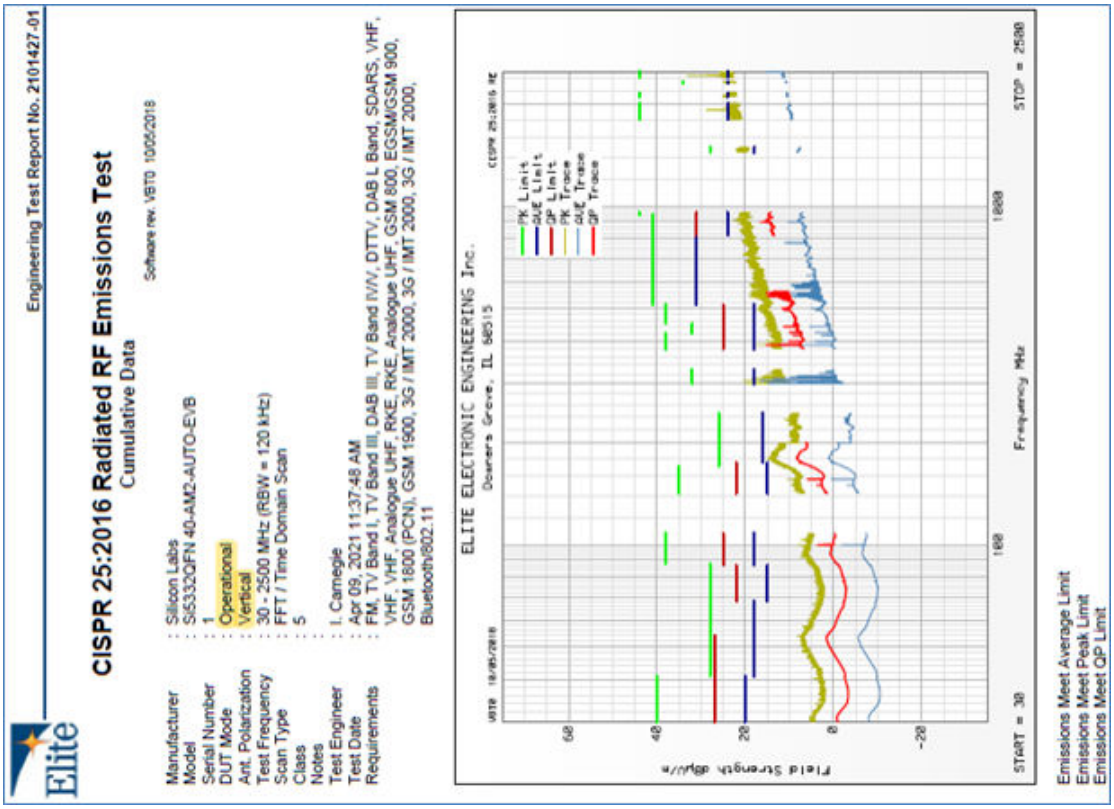


Figure 7.5. DUT Operational - Vertical RF Emissions

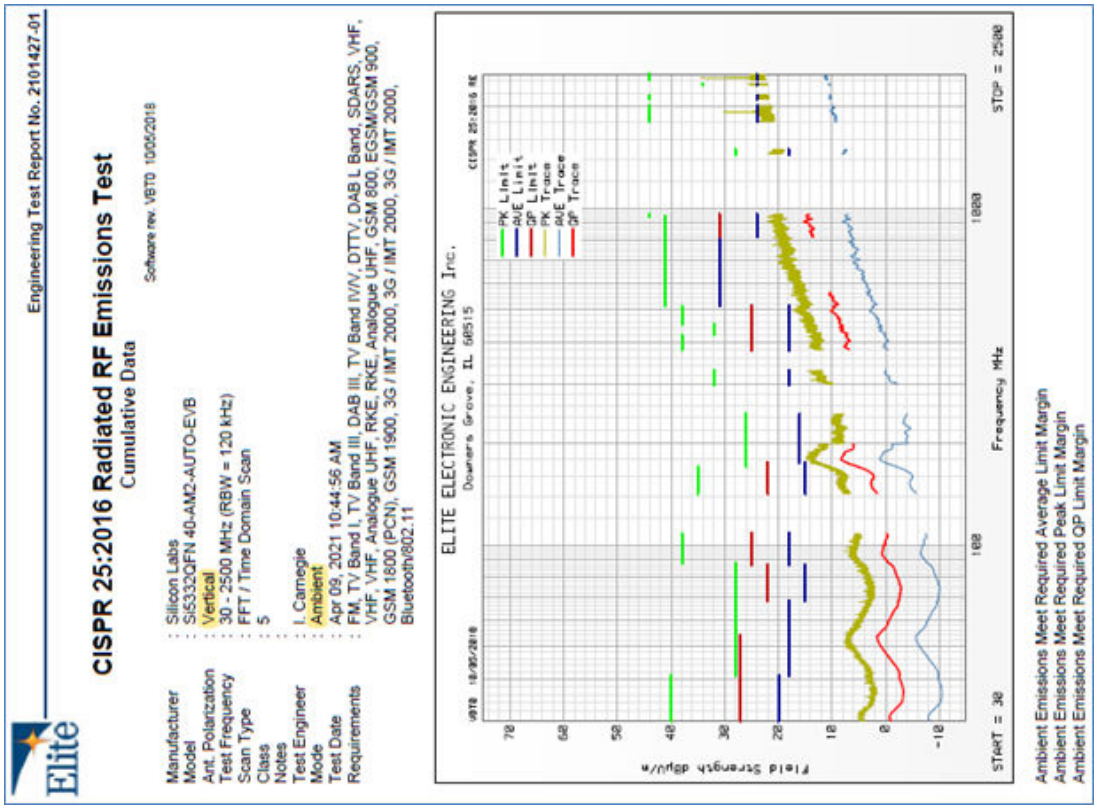


Figure 7.6. DUT Power Off - Background Vertical RF

7.2 Conducted Emissions Test Results

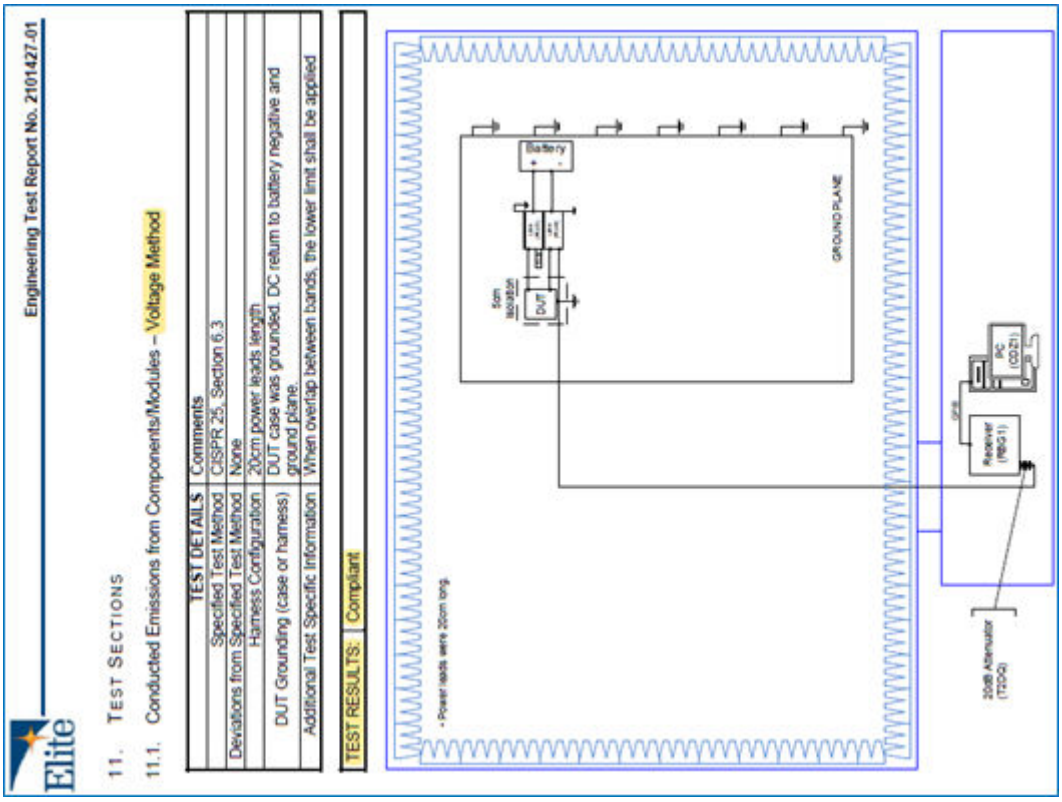


Figure 7.7. Conducted Emissions – Voltage Method

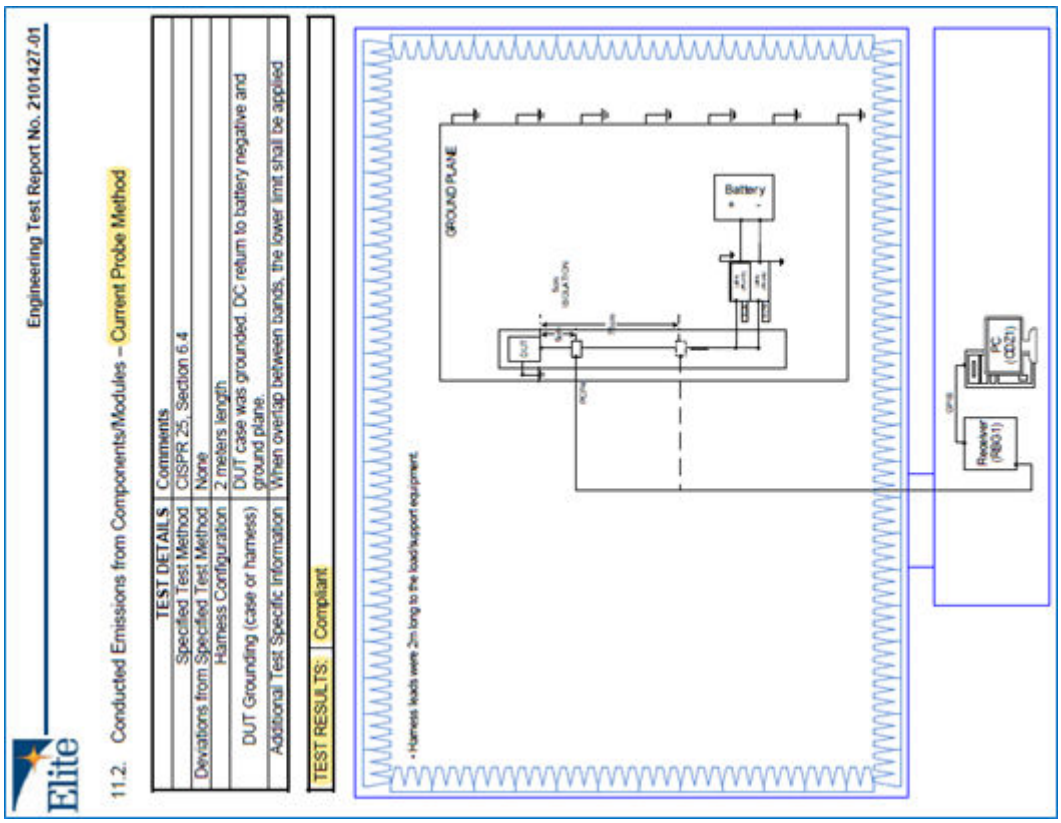


Figure 7.8. Conducted Emissions – Current Method

8. Conclusion

The passing CISPR 25 Class 5 test results presented here support the conclusion that clocks from a central source, such as the Si5332 clock generator, can be routed across a board to multiple destinations in a manner supporting regulatory EMI compliance and even stringent CISPR 25 Class 5 compliance. Following the clock circuit design guidelines and PCB layout design guidelines explained in this application note is the key to achieving product EMI compliance goals.

9. Appendix—Prior EMI Test Data Demonstrating Effectiveness of Suggested EMI Techniques

This appendix describes EMI lab testing done to quantify the real-world EMI performance improvements of the techniques suggested in sections 2 through 5 of this AN1237 document. The testing described in this appendix was done before the full CISPR Class 5 testing shown in section 7 but was later proved crucial to the successful CISPR 25 Class 5 testing. Specifically, the goal of this initial testing was to provide real-world test data on the design techniques required to minimize overall radiated emissions when using a clock generator-based design.

To accomplish this goal, we used the Si5332QFN40-AM2-AUTO-EVB board and did EMI testing with three different output clock profiles. The profiles used for this initial testing are shown below.

Figure 9.1. Frequency Profiles

Profile #1 is an all single-ended LVCMOS clock profile. Profile #2 simply replaces the same clocks in profile #1 with complementary LVCMOS clocks, at exact same frequency. Profile #3 was then added as a mixed profile containing both complementary LVCMOS and traditional differential clocks.

Due to test lab limitations, CISPR 25 Class 4 EMI limits were used instead of Class 5. Since the goal of this testing was to quantify and validate the performance changes, or deltas, between the 3 different profiles this was acceptable for our purposes. Emissions data was collected in physical configurations including open enclosure (top open, board facing antenna) as well as totally closed enclosure to quantify both the emissions from the board itself as well as the added attenuation provided by a simple enclosure.

For capturing the first EMI test plot, profile #1 is used (single-ended LVCMOS profile) with the enclosure top cover open. Below are the radiated emissions for this configuration. Spurs are evidently present although only a few are exceeding Class 4 average spec levels, with none exceed the peak spec levels. Remember, these are single ended LVCMOS clocks contained in an embedded Stripline “cavity” within the PCB. Spur levels would probably be much higher if these clocks were instead on a surface layer of the board.

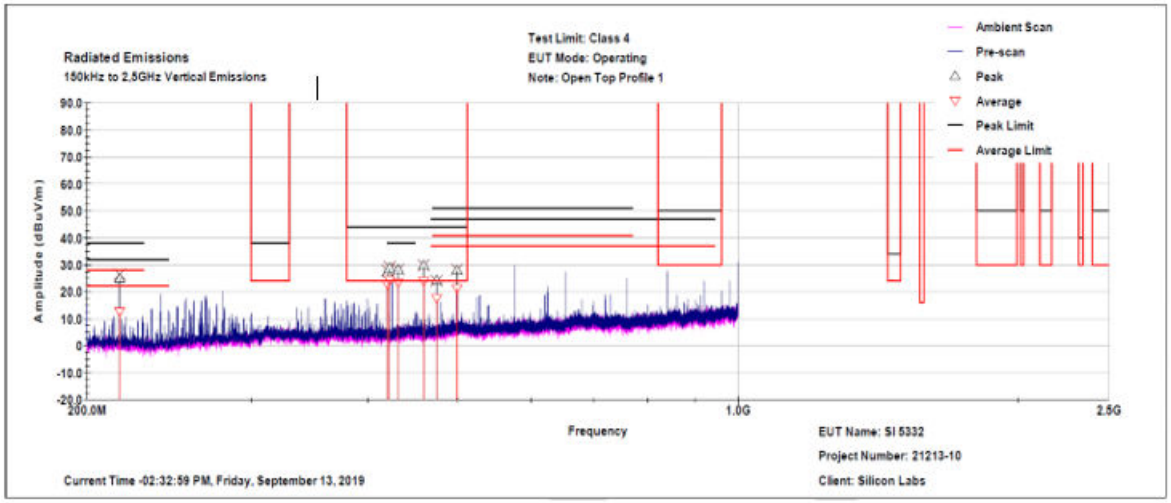


Figure 9.2. Single-Ended LVCMOS Emissions with Stripline PCB

Below is the EMI plot for profile #2 (complementary LVCMOS profile) with enclosure top open as well. Note the marked reduction in radiated spur amplitude (about 10 dB lower) due to changing to complementary LVCMOS. All DUT mid-band generated spurs are well below limits with a single lower frequency spur that is now well below both peak (black levels) and average (red levels) limits.

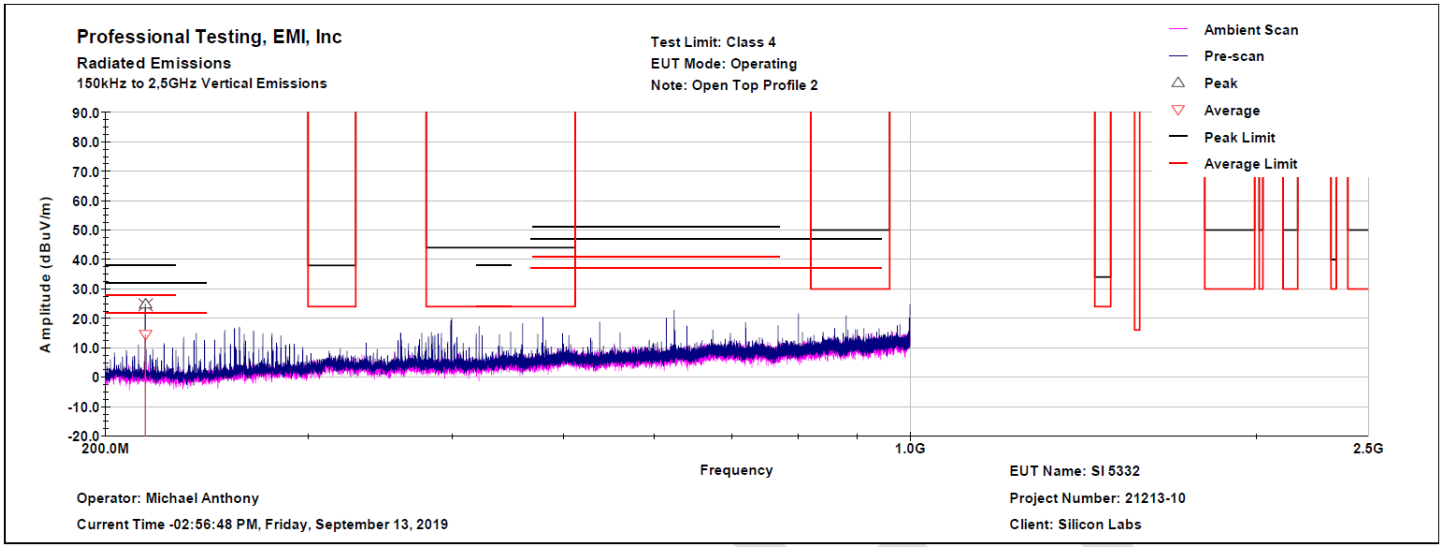


Figure 9.3. Complementary LVCMOS Emissions with Stripline PCB

Below is profile #3 (mixed complementary LVCMOS and differential clocks) with enclosure top open. DUT spurs are also well below limits with lower frequency spur much lower in amplitude. This would easily pass Class 4 limits (with ~20 db margin) without the enclosure top cover on.

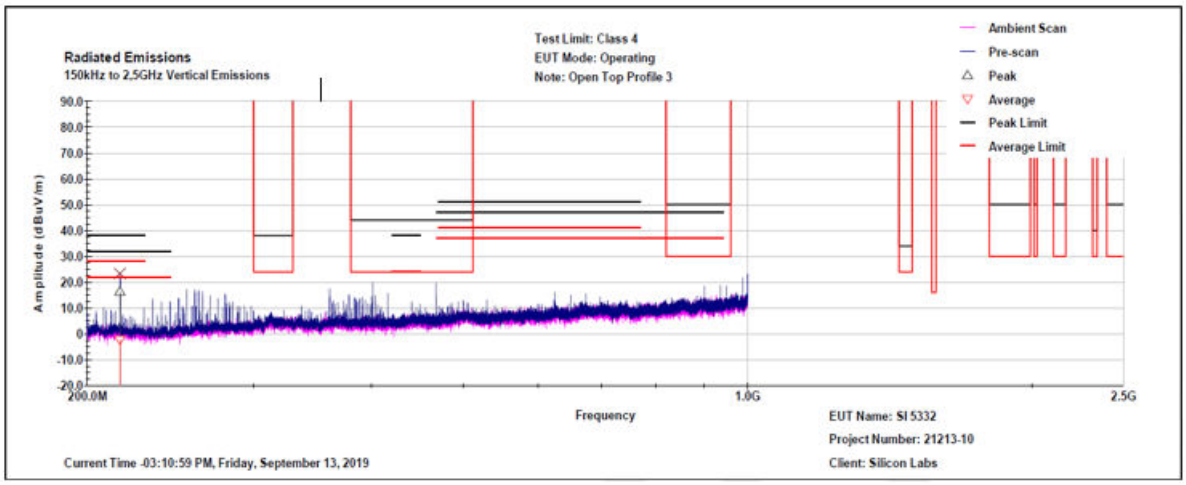


Figure 9.4. Mixed Complementary LVCMOS + Differential Clock Emissions with Stripline PCB

Further EMI testing was done with profile #3 with enclosure top closed. This DUT configuration is most representative of an enclosed automotive assembly undergoing EMI testing. Note the improvement (additional ~ 10 dB) from previous plot once the enclosure top is closed.

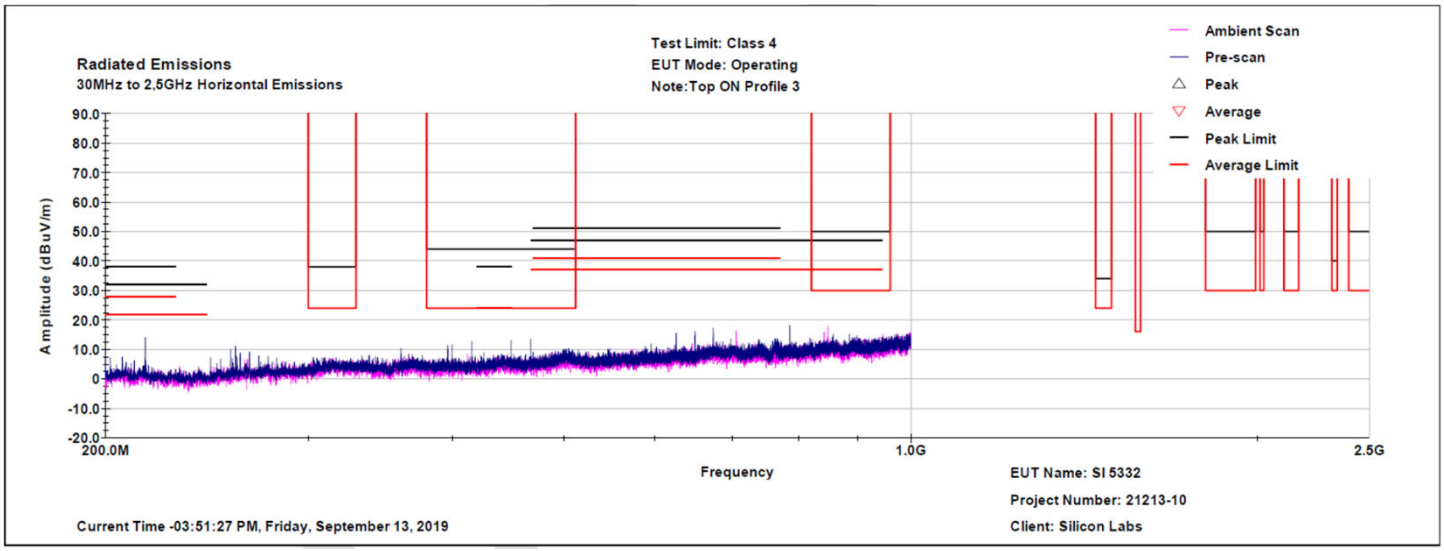


Figure 9.5. Mixed Complementary LVCMOS + Differential Clock Emissions with Stripline PCB and Enclosure Top Closed

Finally, below is the captured spectral emission data for same DUT configuration as shown in above Figure A.5, swept over 1.0 GHz to 2.5 GHz range. Note the lack of spurious emissions above 1 GHz.

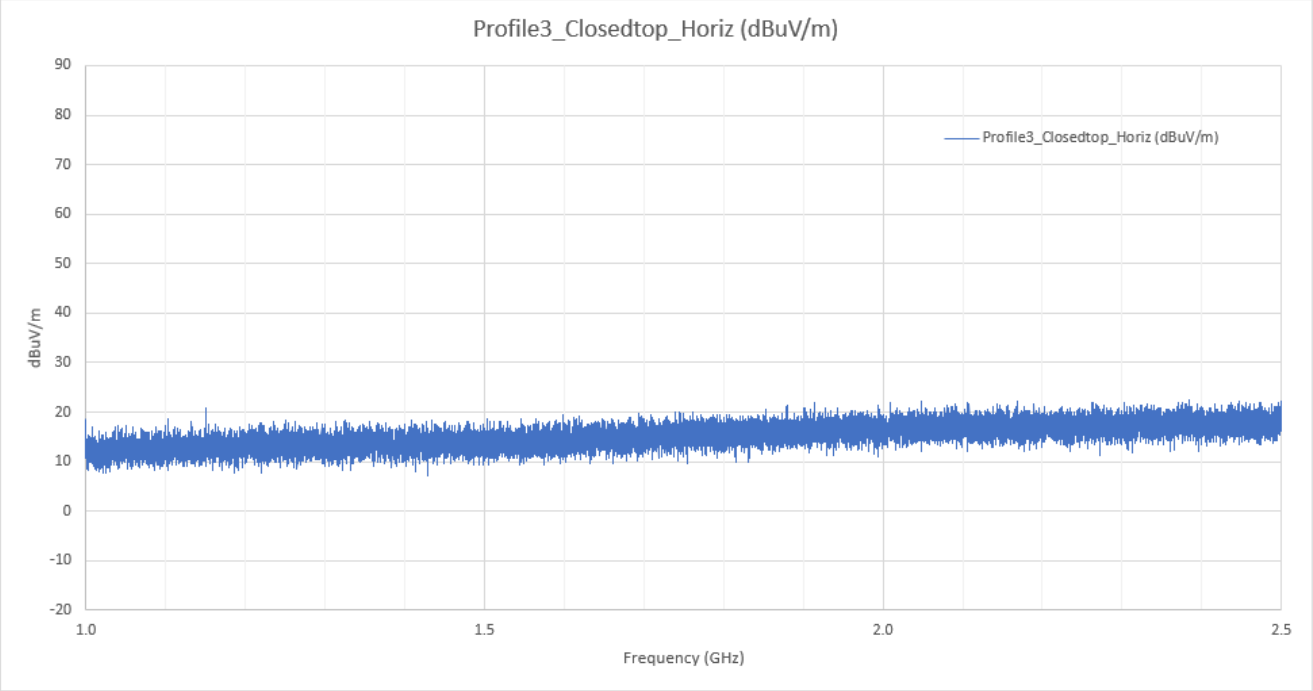


Figure 9.6. Profile #3 from 1GHz to 2.5 GHz, enclosure top closed

The net result of the initial EMI testing described in this appendix provided the following real-world confirmations:

- Stripline routing of clocks does provide valuable EMI reduction.
- Stripline routing coupled with complementary LVCMOS can provide even greater EMI reduction for LVCMOS clocks.
- Introduction of traditional high-speed differential clocks into the clock mix has minimal additional impact on EMI if above two guidelines are followed.
- Following the EMI reduction techniques described in this AN1237 document will increase the likelihood of successful EMI regulatory compliance testing.

SKYWORKS®

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro

Portfolio
www.skyworksinc.com/ia/timing

SW/HW
www.skyworksinc.com/CBPro

Quality
www.skyworksinc.com/quality

Support & Resources
www.skyworksinc.com/support

Skyworks Solutions, Inc. | Nasdaq: SWKS | sales@skyworksinc.com | www.skyworksinc.com
USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540 |